In the Claims

Claims 1-25 (cancelled).

26. (previously presented) A capacitor construction comprising a first capacitor electrode over a substrate, a capacitor dielectric layer over the first electrode, a second capacitor electrode over the dielectric layer, and an atomic layer deposited conductive barrier layer to oxygen diffusion between the first and second electrodes, the dielectric layer being over the barrier layer.

27. (cancelled).

28. (previously presented) The construction of claim 26 further comprising another conductive barrier layer to oxygen diffusion over the dielectric layer.

29. (original) The construction of claim 26 wherein the barrier layer comprises WN, WSiN, TaN, TiN, TiSiN, Pt, Pt alloys, Ir, Ir alloys, Pd, Pd alloys, RuO_x, or IrO_x.

30. (original) The construction of claim 26 wherein the dielectric layer exhibits a K factor of greater than about 7 at 20° C.

31. (previously presented) A capacitor construction comprising:

a first capacitor electrode over a substrate;

a conductive barrier layer to oxygen diffusion over the first electrode, the barrier layer comprising a chemisorption product of first and second precursor layers;

a capacitor dielectric layer over the barrier layer; and

a second capacitor electrode over the dielectric layer.

32. (original) The construction of claim 31 wherein the barrier layer comprises WN, WSiN, TaN, TiN, TiSiN, Pt, Pt alloys, Ir, Ir alloys, Pd, Pd alloys, RuO_x, or IrO_x.

33. (original) The construction of claim 31 wherein the dielectric layer exhibits a K factor of greater than about 7 at 20° C.

34. (previously presented) The construction of claim 26 wherein the barrier layer consists of Pd or Pd alloys.

35. (previously presented) The construction of claim 26 wherein the barrier layer comprises a plurality of atomic layer deposited monolayers.

36. (previously presented) The construction of claim 31 wherein the first and second precursor layers each comprise one atomic layer deposited monolayer.

37. (previously presented) A capacitor construction comprising:

a first capacitor electrode over a substrate;

a conductive barrier layer to oxygen diffusion over the first electrode, the barrier layer comprising Pd or Pd alloys as a chemisorption product of first and second precursor layers;

a capacitor dielectric layer over the barrier layer; and

a second capacitor electrode over the dielectric layer.

38. (previously presented) A capacitor construction comprising a first capacitor electrode over a substrate, a capacitor dielectric layer over the first electrode, a second capacitor electrode over the dielectric layer, and an atomic layer deposited metal-containing conductive layer between the first electrode and dielectric layer.

39. (previously presented) The construction of claim 38 wherein the atomic layer deposited conductive layer is on the first electrode.

40. (previously presented) The construction of claim 38 wherein the atomic layer deposited conductive layer comprises elemental metal, a metal alloy, or a metal-containing compound.

41. (previously presented) The construction of claim 38 wherein the atomic layer deposited conductive layer comprises WN, WSiN, TaN, TiN, TiSiN, Pt, Pt alloys, Ir, Ir alloys, Pd, Pd alloys, RuO_x, or IrO_x.

42. (previously presented) The construction of claim 38 wherein at least one of the first or second electrode comprises polysilicon and the dielectric layer comprises oxygen.

43. (previously presented) A capacitor construction comprising:

a first capacitor electrode over a substrate;

a layer of a metal-containing conductive material over the first electrode, the material comprising a chemisorption product of first and second precursor layers;

a capacitor dielectric layer over the conductive layer; and

a second capacitor electrode over the dielectric layer.

44. (previously presented) The construction of claim 43 wherein the first and second precursor layers each consist essentially of a monolayer.

45. (previously presented) The construction of claim 43 wherein the first and second precursors respectively comprise only one of the following pairs: WF_6/NH_3, $TaCl_5/NH_3$, $TiCl_4/NH_3$, tetrakis(dimethylamido)titanium/NH_3, ruthenium cyclopentadiene/H_2O, IrF_5/H_2O, organometallic Pt/H_2O.

46. (previously presented) The construction of claim 43 wherein the conductive layer is on the first electrode.

47. (previously presented) The construction of claim 43 wherein the conductive layer comprises elemental metal, a metal alloy, or a metal containing compound.

48. (previously presented) The construction of claim 43 wherein the conductive material comprises WN, WSiN, TaN, TiN, TiSiN, Pt, Pt alloys, Ir, Ir alloys, Pd, Pd alloys, RuO_x, or IrO_x.

49. (previously presented) The construction of claim 43 wherein at least one of the first or second electrode comprises polysilicon and the dielectric layer comprises oxygen.

50. (previously presented) The construction of claim 26 wherein the substrate comprises a semiconductive wafer.

51. (previously presented) The construction of claim 26 wherein the first capacitor electrode comprises HSG polysilicon.

52. (previously presented) The construction of claim 51, wherein the atomic layer deposited barrier layer comprises TiN and the first capacitor electrode further comprises the TiN.

53. (previously presented) The construction of claim 26 wherein the atomic layer deposited barrier layer comprises TiN.

54. (previously presented) The construction of claim 26 wherein the capacitor dielectric layer comprises Al_2O_3.

55. (previously presented) The construction of claim 26 wherein the second capacitor electrode comprises TiN.

56. (previously presented) The construction of claim 26 wherein the first capacitor electrode comprises HSG polysilicon, the atomic layer deposited barrier layer comprises TiN, the capacitor dielectric layer comprises Al_2O_3, and the second capacitor electrode comprises TiN.

57. (previously presented) The construction of claim 31 wherein the substrate comprises a semiconductive wafer.

58. (previously presented) The construction of claim 31 wherein the first capacitor electrode comprises HSG polysilicon.

59. (previously presented) The construction of claim 58, wherein the barrier layer comprises TiN and the first capacitor electrode further comprises the TiN.

60. (previously presented) The construction of claim 31 wherein the barrier layer comprises TiN.

61. (previously presented) The construction of claim 31 wherein the capacitor dielectric layer comprises Al_2O_3.

62. (previously presented) The construction of claim 31 wherein the second capacitor electrode comprises TiN.

63. (previously presented) The construction of claim 31 wherein the first capacitor electrode comprises HSG polysilicon, the barrier layer comprises TiN, the capacitor dielectric layer comprises Al_2O_3, and the second capacitor electrode comprises TiN.

64. (previously presented) The construction of claim 38 wherein the substrate comprises a semiconductive wafer.

65. (previously presented) The construction of claim 38 wherein the first capacitor electrode comprises HSG polysilicon.

66. (previously presented) The construction of claim 65, wherein the atomic layer deposited conductive layer comprises TiN and the first capacitor electrode further comprises the TiN.

67. (previously presented) The construction of claim 38 wherein the atomic layer deposited conductive layer comprises TiN.

68. (previously presented) The construction of claim 38 wherein the capacitor dielectric layer comprises Al_2O_3.

69. (previously presented) The construction of claim 38 wherein the second capacitor electrode comprises TiN.

70. (previously presented) The construction of claim 38 wherein the first capacitor electrode comprises HSG polysilicon, the atomic layer deposited conductive layer comprises TiN, the capacitor dielectric layer comprises Al_2O_3, and the second capacitor electrode comprises TiN.

71. (previously presented) The construction of claim 43 wherein the substrate comprises a semiconductive wafer.

72. (previously presented) The construction of claim 43 wherein the first capacitor electrode comprises HSG polysilicon.

73. (previously presented) The construction of claim 72, wherein the conductive layer comprises TiN and the first capacitor electrode further comprises the TiN.

74. (previously presented) The construction of claim 43 wherein the conductive layer comprises TiN.

75. (previously presented) The construction of claim 43 wherein the capacitor dielectric layer comprises Al_2O_3.

76. (previously presented) The construction of claim 43 wherein the second capacitor electrode comprises TiN.

77. (previously presented) The construction of claim 43 wherein the first capacitor electrode comprises HSG polysilicon, the conductive layer comprises TiN, the capacitor dielectric layer comprises Al_2O_3, and the second capacitor electrode comprises TiN.

78. (new) The construction of claim 43 wherein the material comprises a barrier layer to oxygen diffusion.